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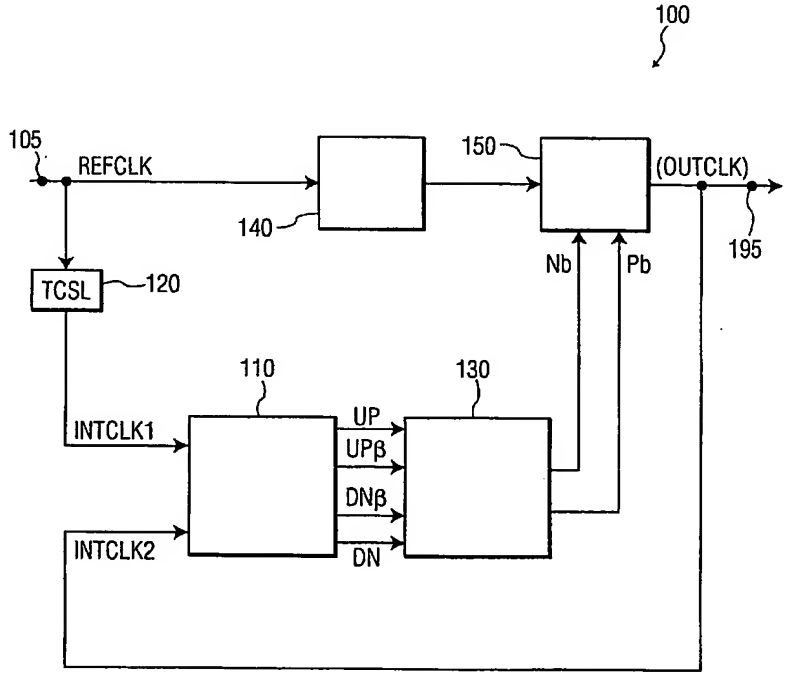
(54) Title: LOW LOCK TIME DELAY LOCKED LOOPS USING TIME CYCLE SUPPPRESSOR



(57) Abstract: The invention discloses a delay locked loop (DLL) architecture with a time cycle suppressor circuit suitable for use with synchronous integrated circuits containing a clock generator. Utilization of the improved delay locked loop architecture with a time cycle suppressor circuit disclosed herein enables reduction in the lock time of the synchronous circuit.

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